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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/643,776

08/19/2003

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EXAMINER

WILLIS, RANDAL L

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/643,776	Applicant(s) OUCHI ET AL.	
	Examiner Randal L. Willis	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2003.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/19/03</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to application No. 10/643776 filed August 19<sup>th</sup> 2003. Claims 1-10 are pending and have been examined.

#### ***Priority***

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Information Disclosure Statement***

3. The information disclosure statement (IDS) submitted on 8/19/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

#### ***Drawings***

4. Figures 8 and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in

the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1,2,4,5,7,9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishizuka 6,731,276.

Apropos claim 1, Ishizuka teaches:

An image display device comprising an electric current-driven electro optic display element (Col 1 lines 10-11) and a drive circuit (Data driver 28, Fig. 3) to control a driving current supplied to said electro optic display element (15, Fig. 5) on a substrate on which a plurality of picture elements is aligned in a form of a matrix (Matrix of pixels 10, Fig. 6) wherein each picture

element has a light-emitting layer that has a transparent picture element electrode (anode 47 Fig. 5) and a metal picture element electrode (cathode of 15, Col 5 lines 20-26) there between to compose the electric current-driven electro optic display element, wherein;

each picture element has a driving circuit (FET 11, Fig. 1 Col 5 line 15) which is connected to a vertical scanning circuit that includes a sequential circuit (Scan driver 27, Fig. 3) through a scanning wire (Scan line Ai, Fig. 1) and to a horizontal driver (Data driver 28, Fig. 3) through a data wire (Data line Bj, Fig. 1), and

either the transparent picture element electrode or the metal picture element electrode (strip electrode 45, Fig. 5) is connected to a wire placed in parallel to said scanning wire (See Fig. 6, 45 parallel to A1) and a terminal of said wire is, through a switching device (S1 Fig. 6), selectively connected to an electric power source (connects to Vg, Vb or Vd, Fig. 6) that gives an electric potential for a purpose of applying a voltage necessary to drive said electric current-driven electro optic display element or to another electric power source that gives an electric potential of which polarity is reverse to a voltage applied in emitting operation (Col 6 line 29-37).

Apropos claim 2, Ishizuka teaches:

An image display device according to Claim 1, wherein said switching device (S1, Fig. 6) has a switching operation by using a sequential circuit (sequentially controlled by Timing control signal Fig. 6) that has a same scanning direction as a same scanning direction that said vertical scanning circuit has (See sequential scanning of scanline and strip electrode for Reverse Bias shown in Fig. 10).

Apropos claim 4, Ishizuka teaches:

An image display device according to Claim 1, wherein either said transparent picture element electrode or said metal picture element electrode is directly or, through a driving device, connected to said wire (Col 5 lines 23-27).

Apropos claim 5, Ishizuka teaches:

An image display device according to Claim 1, wherein;

said switching device (35, Fig. 6) has a switching operation by using a sequential circuit (controller 26, Fig. 3) that has a same scanning direction as a same scanning direction that said vertical scanning circuit has (Fig. 10, reverse bias of strip electrode from switching device scanned same direction as scan signal), and

either said transparent picture element electrode or said metal picture element electrode is directly or, through a driving device, connected to said wire (Col 5 line 20-25).

Apropos claim 7, Ishizuka teaches:

An image display device according to Claim 1, wherein either said transparent picture element electrode or said metal picture element electrode is connected to said wire within each said picture element (Col 5 line 20-25).

Apropos claim 9, Ishizuka teaches:

An image display device comprising:

a plurality of scanning wires (Scan line A1-An, Fig. 6) that are distributively laid over an image display area therein and that transmit a scanning signal there through,

a plurality of data wires (Data Line B1-Bm, Fig. 6) that are laid over said image display area with crossing over the plurality of the scanning wires and that transmit a signal voltage therethrough,

a plurality of electric current-driven electro optic display elements (15 Fig 1) of which each element is laid in each of picture element areas

surrounded by said scanning wire and said data wire and connected to a common electric power supply (Powers supply 36, Fig 3),

a plurality of driving devices (Scan driver 27 Fig. 3) that are connected to said electric current-driven electro optic display elements in series and to a common electric power supply (Voltage VD of power supply 36, Fig. 3) and that activate said electric current-driven electro optic display elements for emission by applying bias voltage thereto (Col 4 lines 30-36), and

a plurality of memory control circuits (Capacitor 13, Fig. 1) that hold said signal voltage in response to said scanning signal and control a driving operation of said driving devices by using said signal voltage (Col 1 line 64-67), wherein;

said memory control circuit holds a signal voltage obtained by a signal sampling (Col 1 line 64-67) with blocking the bias voltage applied to said driving device while said electric current-driven electro optic display elements are kept in a voltage status for non-emission and said signal voltage is applied to the driving device as the bias voltage thereafter (Col 6 line 29-37).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:



(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 3,6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka 6,731,276 in view of Kasai 2002/0050962.

Apropos claim 3, Ishizuka fails to explicitly teach; wherein said switching device has a switching operation by using a signal generated by a sequential circuit built in said vertical scanning circuit.

In the same field of reverse biasing EL displays, Kasai teaches using the Vselect scan signals generated by the vertical scanning circuit to control the switches that apply reverse bias to the EL elements in the display ([0077] lines 10-19).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to reference the vertical scanning circuit in the control of the reverse-bias switches to cut down on the circuitry needed to operate the display.

Apropos claim 6, Ishizuka teaches:

An image display device according to Claim 1, wherein;  
either said transparent picture element electrode or said metal picture element electrode is directly or, through a driving device, connected to said wire (Col 5 line 20-25).

However Ishizuka fails to explicitly teach:

said switching device has a switching operation by using a signal generated by a sequential circuit built in said vertical scanning circuit

In the same field of reverse biasing EL displays, Kasai teaches using the Vselect scan signals generated by the vertical scanning circuit to control the switches that apply reverse bias to the EL elements in the display ([0077] lines 10-19).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to reference the vertical scanning circuit in the control of the reverse-bias switches to cut down on the circuitry needed to operate the display.

Apropos claim 10, Ishizuka fails to explicitly teach: wherein said scanning signal is used for said control signal that change the bias voltage applied to the electric current-driven electro optic display elements in a switching manner.

In the same field of reverse biasing EL displays, Kasai teaches using the Vselect scan signals generated by the vertical scanning circuit to control the switches that apply reverse bias to the EL elements in the display ([0077] lines 10-19).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to reference the vertical scanning circuit in the control of the reverse-bias switches to cut down on the circuitry needed to operate the display.

10. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai 2002/0050862 in view of Nakamura 6,628,258.

Apropos claim 8, Kasai teaches:

An image display device comprising an electric current-driven electro optic display element (Abstract line 1-3) and a drive circuit (circuit driving Vdata, Fig. 2) to control a driving current supplied to said electro optic display

element (10, Fig. 2) on a substrate on which a plurality of picture elements is aligned in a form of a matrix ([0004]) wherein each picture element has a light-emitting layer that has a transparent picture element electrode ([0004]) and a metal picture element electrode ([0004]) there between to compose the electric current-driven electro optic display element, wherein;

each picture element has a driving circuit (Tr2, Fig. 2) which is connected to a vertical scanning circuit through a scanning wire (Vsel, Fig. 2) and to a horizontal driver through a data wire (Vdata Fig. 2), and either the transparent picture element electrode or the metal picture element electrode has a switching device (Swich 20, Fig. 2) within each said picture element of which said switching device has a function to selectively switch-on to a current source or to an electric power source that gives an electric potential which has a reverse polarity of a voltage necessary to drive said electric current-driven electro optic display element in emitting operation ([0077]).

However Kasai does not explicitly teach a vertical scanning circuit that includes a sequential circuit.

In the same field of matrix display devices, Nakamura teaches using a sequential circuit such as a shift register in order to deliver the scan line signals to the pixels of the display (Y shift register, Fig. 1).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a shift register as taught by Nakamura for the scan line driving circuit of Kasai in order to provide a simple and cheap mechanism to drive the display elements.

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Ilda 6,961,041 for teaching a similar reverse biasing scheme.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Randal L. Willis whose telephone number is (571) 270-1461. The examiner can normally be reached on Monday to Friday from 7:30am to 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RLW

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